ANALOG DEVICES

Low Cost Analog Multiplier

AD633

FEATURES

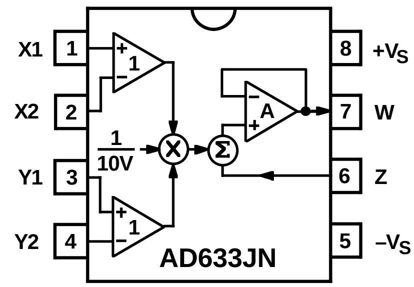
Four-Quadrant Multiplication
Low Cost 8-Pin Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

APPLICATIONS

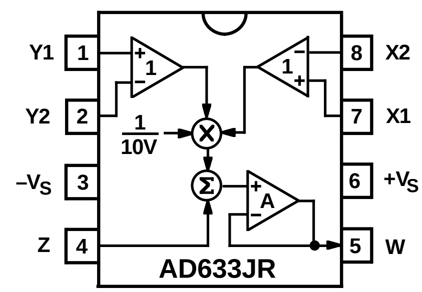
Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/Filters

CONNECTION DIAGRAMS

8-Pin Plastic DIP (N) Package



8-Pin Plastic SOIC (R) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-pin plastic DIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 µV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/µs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

The AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0°C to +70°C commercial temperature range.

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-pin plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

REV. A

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AD633–SPECIFICATIONS (T_A = + 25°C, V_S = ±15 V, $R_L \geq$ 2 kΩ)

Model		AD633J			
TRANSFER FUNCTION		$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\,V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	–10 V ≤ X, Y ≤ +10 V		±1	**±2**	% Full Scale
T_{MIN} to T_{MAX}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5	**±50**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms,		1		MHz
Slew Rate	V_O = 20 V p-p		20		V/µs
Settling Time to 1%	Δ V_O = 20 V		2		µs
OUTPUT NOISE					
Spectral Density			0.8		µV/√Hz
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		µV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	60	80		dB
Bias Current X, Y, Z			0.8	2.0	µA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		**±8**		**±18**	V
Supply Current	Quiescent		4	**6**	mA

NOTES

Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** arc tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . .±18 V
Internal Power Dissipation[2] . . . . 500 mW
Input Voltages[3] . . . .±18 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range . . . . –65°C to +150°C
Operating Temperature Range . . . . 0°C to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C
ESD Rating . . . . 1000 V

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

[2]8-Pin Plastic Package: θ_{JA} = 165°C/W; 8-Pin Small Outline Package: θ_{JA} = 155°C/W.

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

Model	Description	Package Option
AD633JN	8-Pin Plastic DIP	N-8
AD633JR	8-Pin Plastic SOIC	R-8
AD633JR-REEL	8-Pin Plastic SOIC	R-8

FUNCTIONAL DESCRIPTION

The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node. Figure 1 shows the functional block diagram. The differential X and Y inputs are converted to differential currents by voltage-to-current converters. The product of these currents is generated by the multiplying core. A buried Zener reference provides an overall scale factor of 10 V. The sum of (X • Y)/10 + Z is then applied to the output amplifier. The amplifier summing node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computational functions.

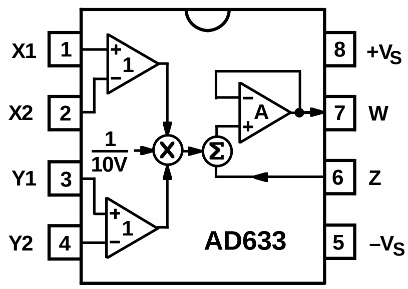


Figure 1. Functional Block Diagram (AD633JN Pinout Shown)

Inspection of the block diagram shows the overall transfer function to be:

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z \qquad \text{(Equation 1)}$$

ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor error, and nonlinearity in the multiplying core. The input and output offsets can be eliminated by using the optional trim of Figure 2. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.4% and 0.1% of full scale, respectively. Scale factor error is typically 0.25% of full scale. The high impedance Z input should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential X and Y inputs should be referenced to their respective grounds to realize the full accuracy of the AD633.

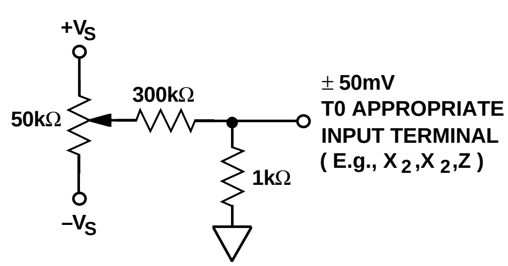


Figure 2. Optional Offset Trim Configuration

APPLICATIONS

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage controlled amplifiers, and frequency doublers. Note that these applications show the pin connections for the AD633JN pinout (8-pin DIP), which differs from the AD633JR pinout (8-pin SOIC).

Multiplier Connections

Figure 3 shows the basic connections for multiplication. The X and Y inputs will normally have their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

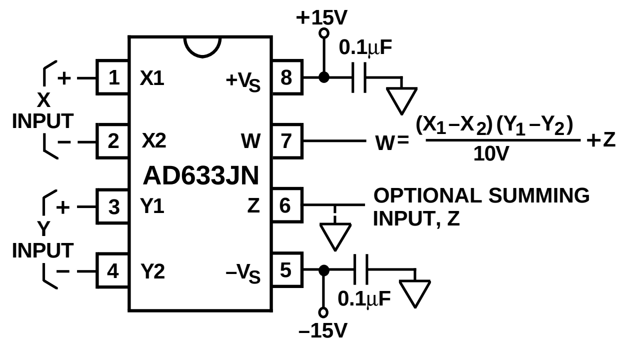


Figure 3. Basic Multiplier Connections

Squaring and Frequency Doubling

As Figure 4 shows, squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input may have either polarity, but the output will be positive. However, the output polarity may be reversed by interchanging the X or Y inputs. The Z input may be used to add a further signal to the output.

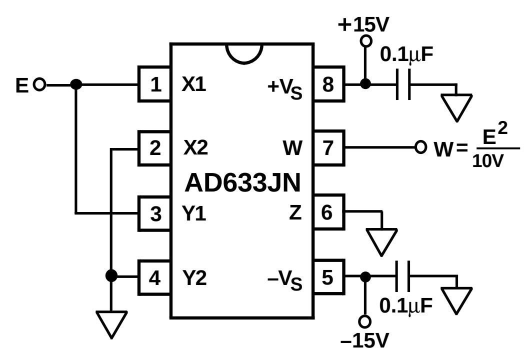


Figure 4. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, since

$$\frac{(E \sin \omega t)^2}{10\ V} = \frac{E^2}{20\ V}(1 - \cos 2\ \omega t) \qquad \text{(Equation 2)}$$

Equation 2 shows a dc term at the output which will vary strongly with the amplitude of the input, E. This can be avoided

using the connections shown in Figure 5, where an RC network is used to generate two signals whose product has no dc term. It uses the identify:

$$\cos\theta\sin\theta = \frac{1}{2}(\sin 2\theta) \qquad \text{(Equation 3)}$$

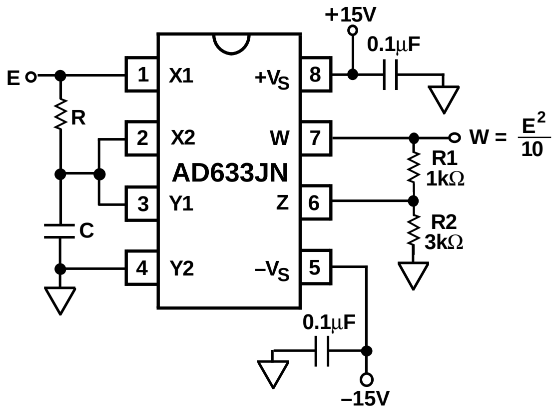


Figure 5. "Bounceless" Frequency Doubler

At $\omega_o = 1/CR$, the X input leads the input signal by 45° (and is attenuated by $\sqrt{2}$), and the Y input lags the X input by 45° (and is also attenuated by $\sqrt{2}$). Since the X and Y inputs are 90° out of phase, the response of the circuit will be (satisfying Equation 3):

$$W = \frac{1}{(10\,V)}\frac{E}{\sqrt{2}}(\sin\omega_o t + 45°)\frac{E}{\sqrt{2}}(\sin\omega_o t - 45°)$$

$$= \frac{E^2}{(40\,V)}(\sin 2\omega_o t) \qquad \text{(Equation 4)}$$

which has no dc component. Resistors R1 and R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.

The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at $\omega = 0.9\,\omega_o$, and $\omega_o = 1.1\,\omega_o$.

Generating Inverse Functions

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 6 shows how to implement a square rooter with the transfer function

$$W = \sqrt{-(10\,V)\,E} \qquad \text{(Equation 5)}$$

for the condition E<0.

Likewise, Figure 7 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W = -(10\,V)\frac{E}{E_X} \qquad \text{(Equation 6)}$$

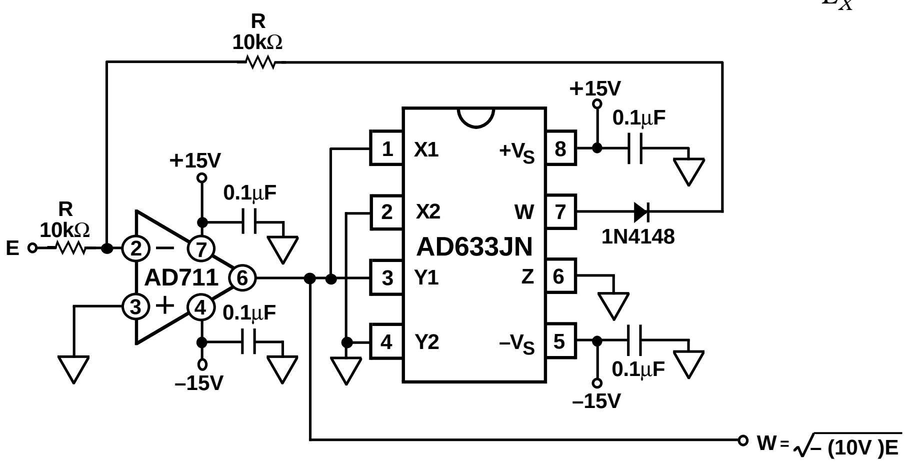


Figure 6. Connections for Square Rooting

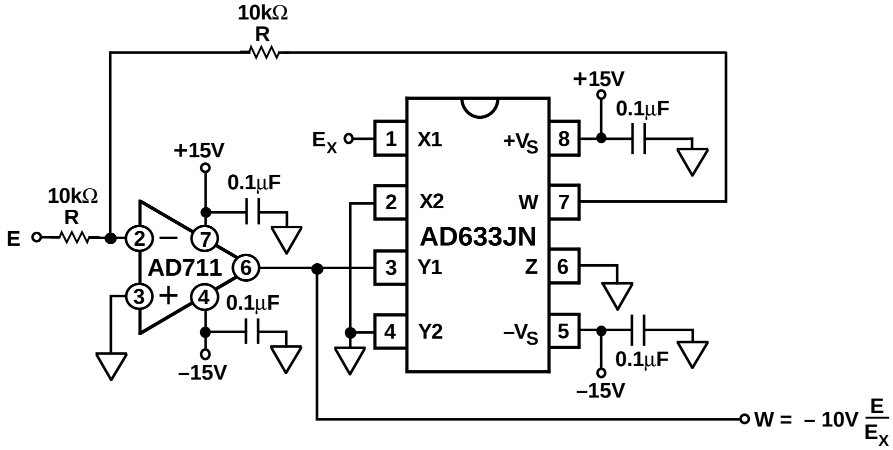


Figure 7. Connections for Division

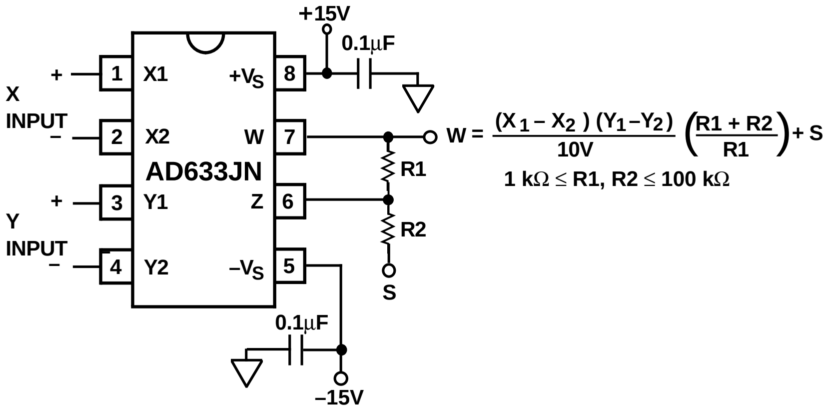


Figure 8. Connections for Variable Scale Factor

Variable Scale Factor

In some instances, it may be desirable to use a scaling voltage other than 10 V. The connections shown in Figure 8 increase the gain of the system by the ratio (R1 + R2)/R1. This ratio is limited to 100 in practical applications. The summing input, S, may be used to add an additional signal to the output or it may be grounded.

Current Output

The AD633's voltage output can be converted to a current output by the addition of a resistor R between the AD633's W and Z pins as shown in Figure 9 below. This arrangement forms the

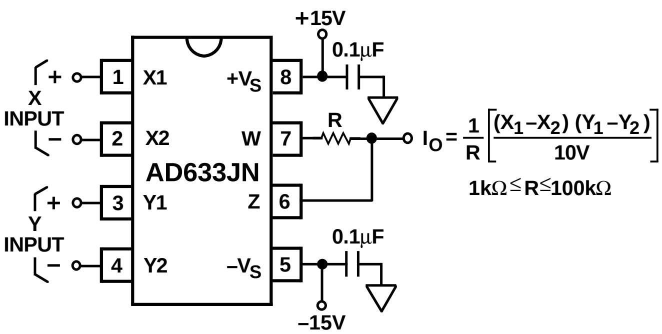


Figure 9. Current Output Connections

basis of voltage controlled integrators and oscillators as will be shown later in this Applications section. The transfer function of this circuit has the form

$$I_O = \frac{1}{R}\frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} \qquad \text{(Equation 7)}$$

Linear Amplitude Modulator

The AD633 can be used as a linear amplitude modulator with no external components. Figure 10 shows the circuit. The carrier and modulation inputs to the AD633 are multiplied to produce a double-sideband signal. The carrier signal is fed forward to the AD633's Z input where it is summed with the double-sideband signal to produce a double-sideband with carrier output.

Voltage Controlled Low-Pass and High-Pass Filters

Figure 11 shows a single multiplier used to build a voltage controlled low-pass filter. The voltage at output A is a result of filtering, E_S. The break frequency is modulated by E_C, the control input. The break frequency, f_2, equals

$$f_2 = \frac{E_C}{(20\ V)\ \pi\ RC} \qquad \text{(Equation 8)}$$

and the rolloff is 6 dB per octave. This output, which is at a high impedance point, may need to be buffered.

The voltage at output B, the direct output of the AD633, has same response up to frequency f_1, the natural breakpoint of RC filter,

$$f_1 = \frac{1}{2\ \pi\ RC} \qquad \text{(Equation 9)}$$

then levels off to a constant attenuation of $f_1/f_2 = E_C/10$.

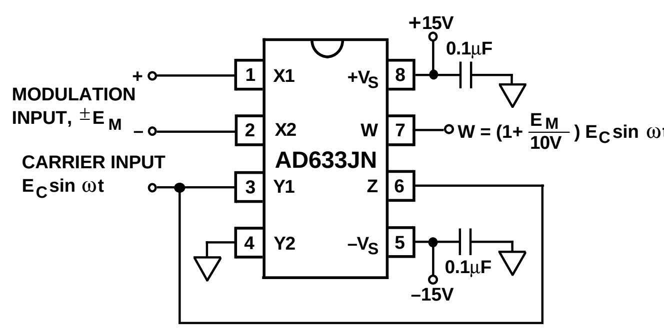


Figure 10. Linear Amplitude Modulator

For example, if R = 8 kΩ and C = 0.002 μF, then output A a pole at frequencies from 100 Hz to 10 kHz for E_C ranging from 100 mV to 10 V. Output B has an additional zero at 10 kHz

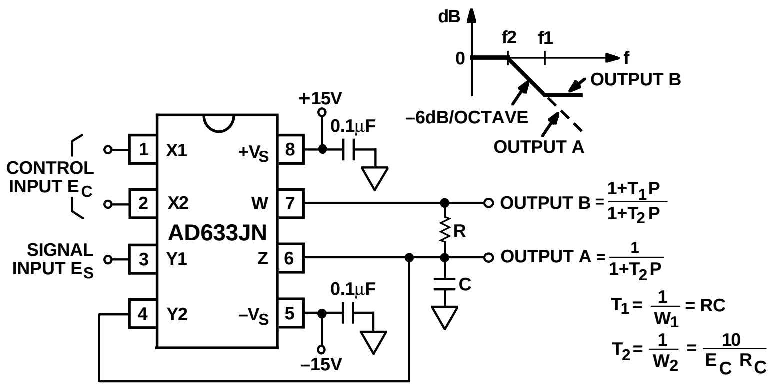


Figure 11. Voltage Controlled Low-Pass Filter

(and can be loaded because it is the multiplier's low impedance output). The circuit can be changed to a high-pass filter Z interchanging the resistor and capacitor as shown in Figure 12 below.

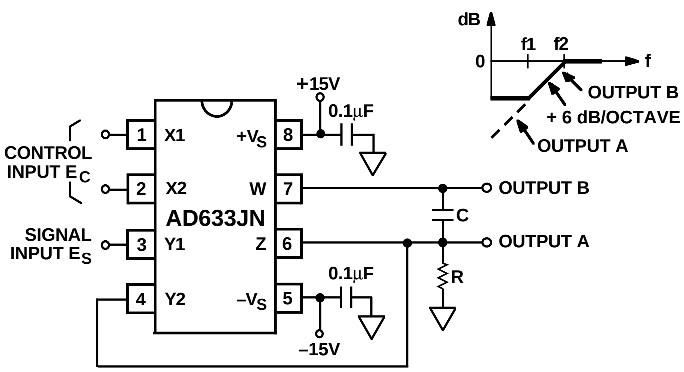


Figure 12. Voltage Controlled High-Pass Filter

Voltage Controlled Quadrature Oscillator

Figure 13 shows two multipliers being used to form integrators with controllable time constants in a 2nd order differential equation feedback loop. R2 and R5 provide controlled current output operation. The currents are integrated in capacitors C1 and C2, and the resulting voltages at high impedance are applied to the X inputs of the "next" AD633. The frequency control input, E_C, connected to the Y inputs, varies the integrator gains with a calibration of 100 Hz/V. The accuracy is limited by the Y-input offsets. The practical tuning range of this circuit is 100:1. C2 (proportional to C1 and C3), R3, and R4 provide regenerative feedback to start and maintain oscillation. The diode bridge, D1 through D4 (1N914s), and Zener diode D5 provide economical temperature stabilization and amplitude stabilization at ±8.5 V by degenerative damping. The output from the second integrator (10 V sin ωt) has the lowest distortion.

AGC AMPLIFIERS

Figure 14 shows an AGC circuit that uses an rms-dc converter to measure the amplitude of the output waveform. The AD633 and A1, 1/2 of an AD712 dual op amp, form a voltage controlled amplifier. The rms dc converter, an AD736, measures the rms value of the output signal. Its output drives A2, an integrator/comparator, whose output controls the gain of the voltage controlled amplifier. The 1N4148 diode prevents the output of A2 from going negative. R8, a 50 kΩ variable resistor, sets the circuit's output level. Feedback around the loop forces the voltages at the inverting and noninverting inputs of A2 to be equal, thus the AGC.

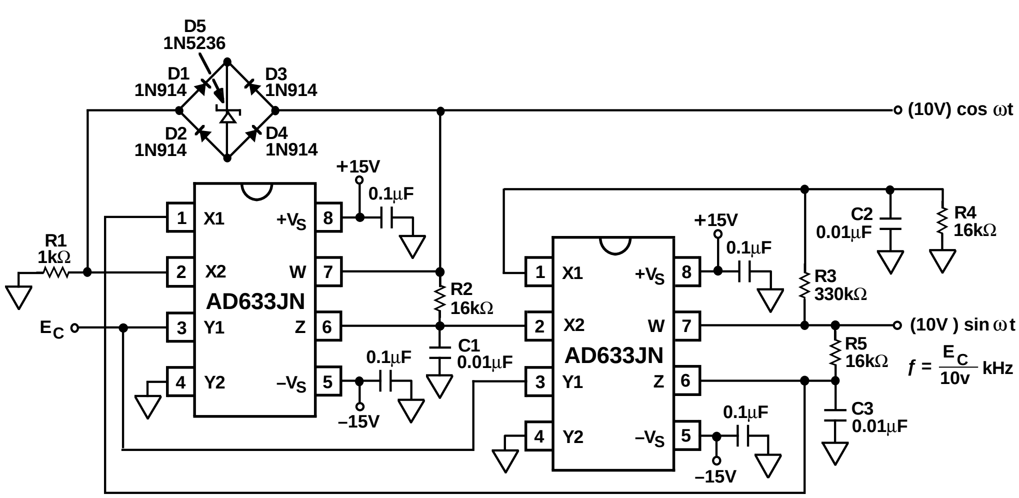


Figure 13. Voltage Controlled Quadrature Oscillator

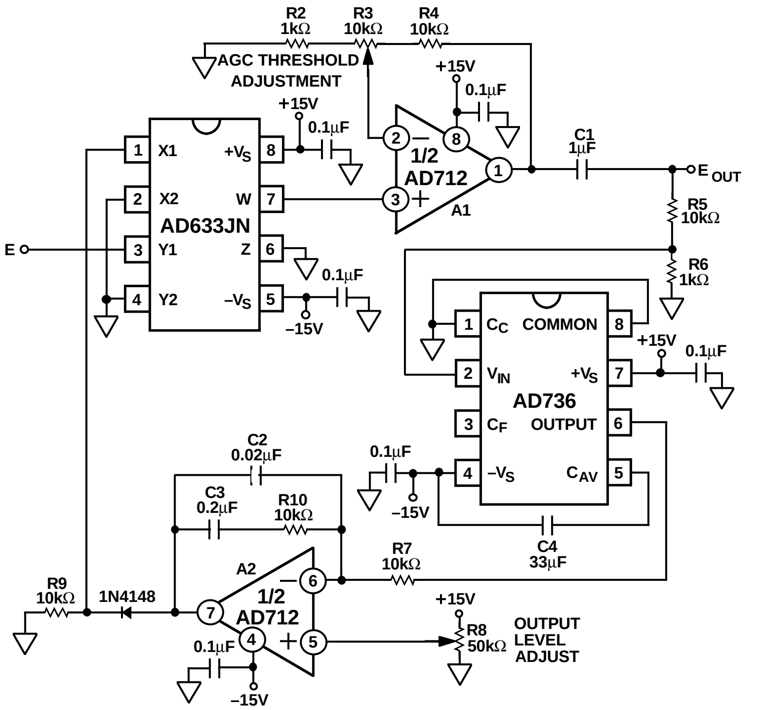


Figure 14. Connections for Use in Automatic Gain Control Circuit

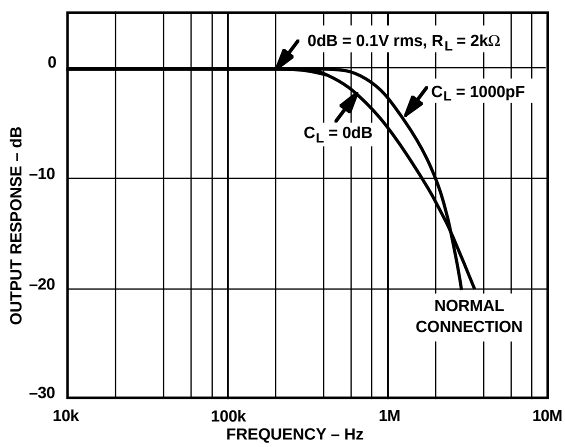


Figure 15. Frequency Response

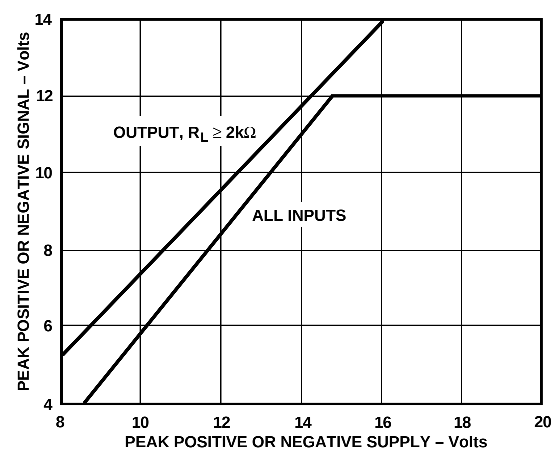


Figure 17. Input and Output Signal Ranges vs. Supply Voltages

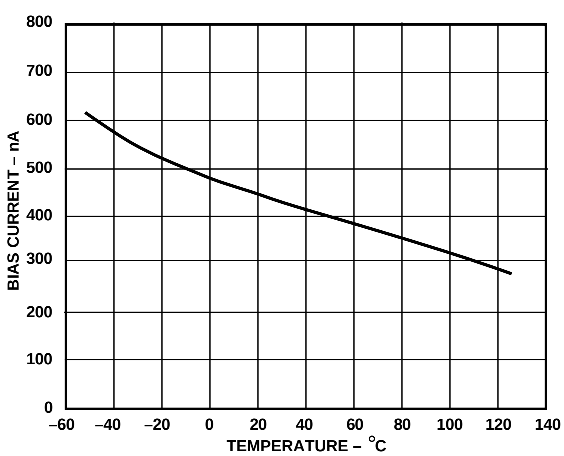


Figure 16. Input Bias Current vs. Temperature (X, Y, or Z Inputs)

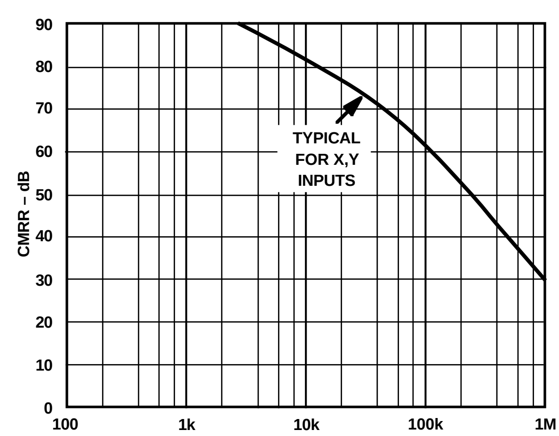


Figure 18. CMRR vs. Frequency

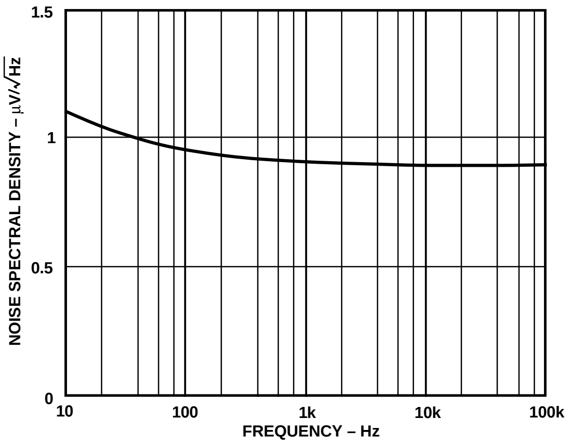


Figure 19. Noise Spectral Density vs. Frequency

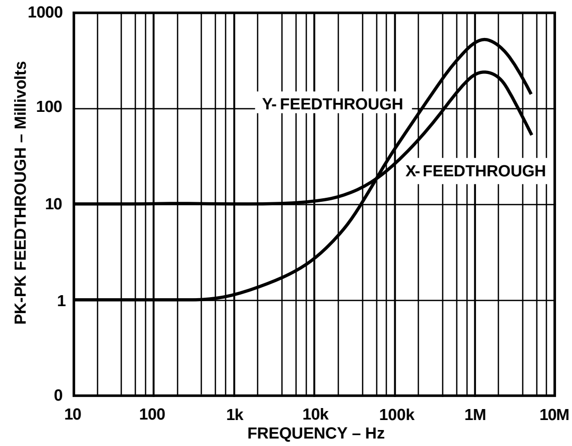
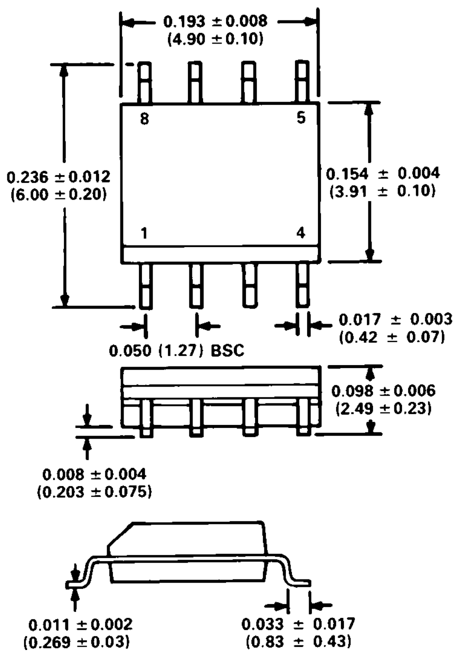


Figure 20. AC Feedthrough vs. Frequency

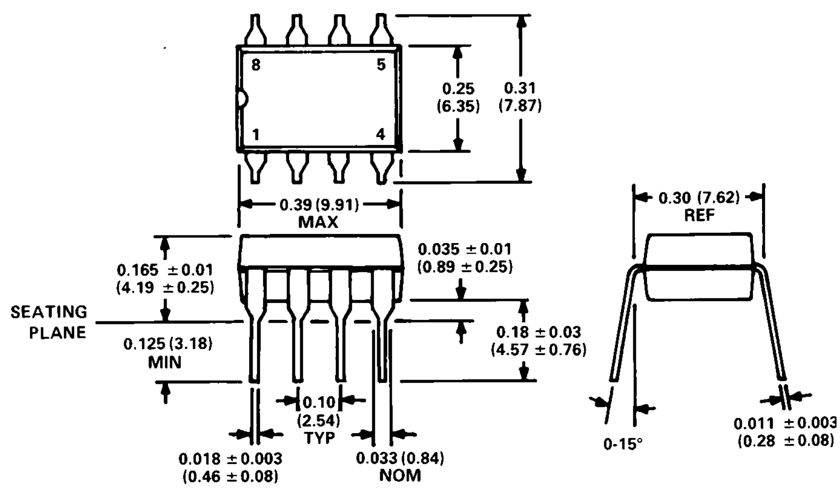
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Pin Plastic SOIC (R) Package



8-Pin Plastic DIP (N) Package



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